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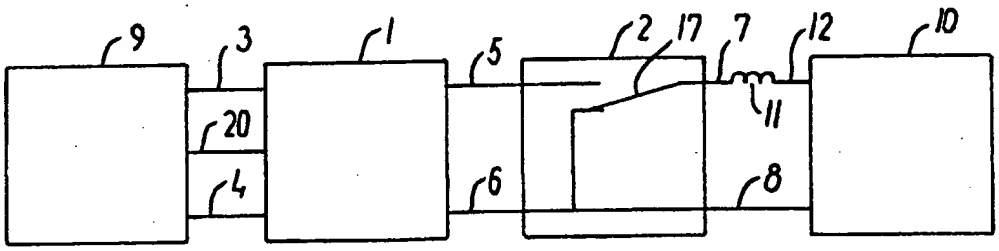

(57) Abstract

With a view to generating minimally distorted square–wave pulses with limited noise and limited peak current during and after the switching sequences in a switched circuit, e.g. a class D amplifier output stage or a power supply, the invention provides a circuit and a method. Seen from one port of the circuit, the short–circuit impedance has a low impedance at low frequencies, while it has a high impedance and is predominantly resistive at high impedances. In one embodiment, the circuit consists of an inductance which is connected between the one and the other ports of the two–port network, and of a series connection of a resistor and a capacitor which is connected between the terminals of the other port of the circuit. The circuit, in combination with a switched circuit, may be formed as an integrated unit on a substrate, where the inductance may advantageously be formed by a conductor path.

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A METHOD OF REDUCING DISTORTION AND NOISE OF SQUARE-WAVE PULSES, A CIRCUIT FOR GENERATING MINIMALY DISTORTED PULSES AND USE OF METHOD AND THE CIRCUIT

The invention relates to a method of reducing distortion and noise of square-wave pulses and of limiting peak currents which occur during the switching sequences in switched circuits of the two-port system, which has a switchable port with a switching terminal capable of being switched between the terminals of a second circuit.

Further, the invention relates to a circuit of the type which, in combination with a switched circuit of the two-port type is capable of generating minimally distorted square-wave pulses with minimum noise and of limiting peak currents which occur during the switching sequences of the square-wave pulses, said switched circuit having a terminal capable of being switched between two terminals of a second circuit.

Finally, the invention relates to uses of the method and the circuit.

Traditional switched circuits for use for power electronics require a certain dead time to avoid great destructive connecting and disconnecting currents, partly to restrict switching losses in the half-bridge incorporated in the circuit and partly to eliminate ringings on the output signal with out adding a parallel snubber and thereby increased losses.

Addition of dead time in switched circuits used in amplifiers and particularly in class D amplifiers for HI-FI, however, involves an intolerable distortion of the modulated output signals. Therefore, it has long been at-

tempted to find a principle which allows dead time in half-bridges to be reduced without bringing about the above-mentioned drawbacks.

The principle of a switched amplifier is that one or more switches in a switched circuit of the two-port type or a multiple thereof is switched to conduct and non-conduct, respectively, e.g. by pulse-width or pulse-density modulation, depending on the amplitude of a signal, such as an audio signal.

Hereby, the information of the audio signal is converted into a number of pulses which exactly correspond to the information of the audio signal.

The primary advantage of pulse-modulated amplifiers is a very high efficiency, which theoretically is 100%, which means that, theoretically, the amplifier has no loss. In practical realisations of pulse-modulated amplifiers, typical efficiencies of between 90 and 98% may be achieved. Pulse-modulated amplifiers are also totally linear in theory and thereby have a very low distortion, but in practice it has been found that non-linearities have caused them to be unsuitable for use in High Fidelity amplifiers for audio. The reason is primarily that it is not possible to provide ideal square-wave pulses in the switched circuit, due to the use og switches that are not ideal having parasitic capacitive and inductive components around the switch element.

One of the main reasons why the pulses cannot be generated ideally is inter alia to be found in the connection and disconnection of the switches. The pulse widths vary as a consequence of variations in the turn-on and turn-off times of the switches, while the necessary dead time between connection and disconnection of the two switches is kept constant. The variations in the turn on and turn off times is due to several factors, among which the most

important is the varying load current and variations in the characteristics of the components used in and around the output stage. The most important variations in the component characteristics is due to variations in temperature but also varying component characteristics due to different batches and eldering phenomena's are known as important issues that must be taken care of. It is therefore desirable to reduce the turn-on and turn-off times and thereby the dead time to a minimum in pulse-modulated power amplifiers.

Conversely, reduced turn-on and turn-off times as well as less dead time causes problems of increased power consumption, and consequent destructive peak currents in the switches and strong ringing on the output signal, as both switches will briefly be turned on simultaneously.

Moreover, it is known that the pulse heights vary because of the ringing which occurs when connecting and disconnecting the load current, which causes distortion of the audio signal.

Such ringing may be partly limited by establishing a parallel snubber circuit of a known type over the switches which attenuates the oscillations that occur because of the parasitic inductance's and capacities of the switching circuit. The drawback of such a circuit, however, is that the turn-on and turn-off times are increased, and that the switching losses and thereby the idle loss of the amplifier are increased, so that the efficiency of the amplifier is reduced and the pulse-width distortion is increased.

Existing practical realisations nevertheless use parallel snubber circuits, as the ringing in and around switched circuits means that the circuits emit so strong high-frequency signals that the circuits cannot be used according to the current standards in the field.

The known methods of generating square-wave pulses in switched amplifiers thus involve distortion of the modulated signal. These methods are particularly not suitable for use in switched amplifiers, e.g. class D amplifiers for HI-FI, where design criteria, such as low distortion, low noise and high efficiency, are important.

There are two categories of switched amplifiers for audio. One category is switched amplifiers having analogue input signals. The other category is switched amplifiers having digital input signals.

The latter amplifier exclusively operates in the digital domain, and is therefore called full digital power amplifier.

Particularly in the full digital power amplifier it is important to be able to generate approximately ideal square-wave pulses, as the distortion-reducing feedback around the output stage cannot be realised, without having to leave the digital domain.

This makes very strict demands on the linearity of the output stage and thereby on the generation of the square-wave pulses with a minimal distortion and noise.

Accordingly, it is an object of the invention to provide a method capable of generating minimally distorted square-wave pulses with minimum noise and minimum losses in the output stage and of reducing the peak current during the switching sequences in the switched circuit.

The object of the invention is achieved by the method stated in the introductory portion of claim 1, which is characterised in that the terminals of the switched circuit are connected to a set of terminals of the second circuit, and that the second circuit is given a short-

circuit impedance which, seen from the switched circuit, provides a characteristic which has a low impedance at low frequencies, while it has a high impedance and is predominantly resistive at high frequencies.

The circuit thus has the advantage that the high-frequency ringing, which normally occurs because of parasitic inductance's and capacities in the switched circuit, may be attenuated significantly by the resistive damping.

The resistive behaviour of the noise attenuating circuit at high frequencies also has the advantage that transient peak currents in the switched circuit may be reduced to a maximum value event by short-circuit of the switching contacts. The dead time may therefore be reduced to a minimum, without generating destructive current in the switches or pulse height errors in the form of strong ringing on the output signal originating from strong short-circuit currents.

When, as stated in claim 2, a single or double voltage supply is applied to the terminals of the second circuit which are not connected to the switched circuit, and a series coupling of an inductance and a load circuit is applied to the port of the switched circuit containing the switching terminal, it is ensured that a Buck converter may be produced, approximately capable of generating ideal square-wave pulses of minimum distortion and noise in the form of minimum dead time and ringing in the switched circuit, while the peak current in the switches in the switched circuit may be limited to a maximum value.

When, as stated in claim 3, a load circuit is connected to the terminals of the second circuit which are not connected to the switched circuit, and a series coupling of an inductance and a voltage supply is applied to the port

of the switched circuit containing the switching terminal, it is ensured that a Boost converter may be produced, capable of generating approximately ideal square-wave pulses of minimum distortion and noise in the form of minimum dead time and ringing in the switched circuit, while the peak current in the switches of the switched circuit is reduced to a maximum value.

As mentioned, the invention also relates to a circuit.

This circuit is characterized in that the second circuit is formed by a network which, seen from the switched circuit, has a short-circuit impedance which has a low impedance at low frequencies and has a high impedance and is predominantly resistive at high frequencies.

The predominantly resistive impedance at high frequencies provides the advantage that the circuit serves as a current limiter during the transient switching sequences in the switched circuit, thereby allowing a minimum dead time to be maintained. The predominantly resistive behaviour of the noise attenuating circuit at high frequencies additionally has the advantage that the high-frequency ringing which normally occurs because of parasitic inductances and capacities in the switched circuit is attenuated considerably. Compared to parallel snubber circuits where the same can be achieved this circuit has less losses, due to there is no parallel capacitor that must be voltage shifted by the switches.

When, as stated in claim 6, the network comprises an inductive component which is connected to a series connection of a capacitive and a resistive component, a very simple circuit structure having only three components is obtained.

When, as stated in claim 7, a resistive component is connected in parallel with the inductive component, it is

ensured that the value of the resistor in the series coupling of the capacitor and the resistor may be increased, as the two resistors form an AC parallel coupling.

As stated in claim 8, it is expedient that the values of the capacitive and inductive components of the network are at least four times greater than the values of the parasitic capacitive and inductive components of the switched circuit.

When, as stated in claim 9, the resistive value of the network at high frequencies is twice the characteristic impedance of the overall parasitic inductance and the overall parasitic capacity in the switched circuit, a strong attenuation of the inevitably occurring oscillations is achieved, which means that dead time between as well as turn-on and turn-off rates of the switches in the switched circuit may be reduced to a minimum, without the occurrence of strong ringings which would otherwise have caused distortion and noise and possible destruction of the switches.

As stated in claim 10, the distortion of the square-wave pulses may be reduced additionally in that an already known snubber circuit consisting of a series connection of a capacitor and a resistor is connected in parallel with the switch elements in the switched circuit. The circuit exhibits particularly reduced distortion when used in switched circuits having relatively great parasitic inductances. The addition of the parallel snubber circuits may advantageously be performed in switched circuit designs where the characteristic impedance of parasitic inductances and capacities is great, which may occur e.g. in layouts of large dimensions.

As stated in claim 11, the network and the switched circuit are formed as an integrated unit on a substrate.

This means that the parasitic inductances and the distortion in the half-bridge are reduced additionally.

When, as stated in claim 13, the series connection of the capacitor and the resistor of the circuit is formed by a capacitor and its internal series resistance, it is ensured that the circuit may be realized in a very simple manner.

Expedient embodiments of the invention are defined in the dependent claims.

As mentioned, the invention finally relates to uses of the method and the circuit.

These uses are defined in claims 14 and 15.

Thus, in class D amplifiers and power supplies, it is possible to provide a limitation in the peak current in the switches, and a much simpler reduction in noise, distortion and ringing in the switched circuits incorporated therein, than is possible to achieve in traditionally used filterings in switched circuits.

The invention will now be explained more fully with reference to an embodiment of the invention shown in the drawing, in which

fig. 1 shows the basic structure of the invention in block diagram form,

fig. 2 shows examples of uses of the invention in block diagram form,

fig. 3 shows an example of a switched circuit of the two-port type in the fig. 1 basic structure,

fig. 4 shows an example of a two-port network in diagram form in the fig. 1 basic structurè according to the invention,

fig. 5 shows an example of a second circuit in diagram form in the fig. 1 basic structure according to the invention,

fig. 6 shows the course of a voltage in the circuit during and after a switching sequence,

fig. 7 shows a course of a voltage in the circuit which constitutes the invention,

fig. 8 shows an example of a noise attenuating circuit in diagram form in the fig. 1 basic structure,

fig. 9 shows another example of a noise attenuating circuit in diagram form in the fig. 1 basic structure,

fig. 10 shows an example in diagram form of how a single voltage supply may be connected to the noise attenuating circuit,

fig. 11 shows an example in diagram form of how a double voltage supply may be connected to the noise attenuating circuit in the fig. 2 diagram,

fig. 12 shows an example in diagram form of how a load may be connected to the noise attenuating circuit in yhe fig.2 diagram.

fig. 13 shows an example of how the circuits 1 and 2 in fig. 1 may be realised.

fig. 14a - 14g shows different states of current flows in the circuits 1 and 2 showed in figure 13.

fig. 15a - 15b shows different states in current flow of the circuits 1 and 2 at low frequencies.

fig. 16a - 16b shows different states in current flow of the circuits 1 and 2 at very high frequencies.

In figure 1, the numeral 1 designates a circuit which is connected to a switched circuit of the two-port type 2 via two terminals 5 and 6. The switched circuit is formed by a two-port, in which the terminals 6 and 8 are interconnected, and one port accommodates a switching terminal 7 which is connected to a switch 17 capable of being switched between the two terminals 5 and 6 of the other port. The short-circuit impedance (with terminals 3, 4 and 20 short-circuited) of the circuit 1, seen from the port containing the terminals 5 and 6, is characteristic by being low at low frequencies and high and predominantly resistive at high frequencies.

Figure 2 shows examples of the use of the circuit 1 and the switched circuit 2, in which the terminals 3, 4 and 20 of the circuit 1 are connected to a circuit 9, and in which the terminal 7 of the switched circuit is connected to a series coupling of an inductance 11 and a circuit 10 which is connected to the terminal 8. The circuits 9 and 10 may e.g. be given by a voltage supply 9 and a load 10, whereby the circuit 1 and the switched circuit 2 are incorporated in a configuration which is known as a Buck converter from the literature. Correspondingly, the circuits 9 and 10 may be given by a load 9 and a voltage supply 10, whereby the circuit and the switched circuit are incorporated in a configuration which is known as a Boost converter.

Figure 3 shows an example of a simplified switched circuit 2 of the two-port type, in which the parasitic components are also shown. One port accommodates a

switchable terminal 7 which may be switched between the terminals 5 and 6 of the other port of fig.1 or 2. The terminals 6 and 8 of the ports are shown to be interconnected. The parasitic components of the switched circuit are drawn around the switches 34, 35. The parasitic inductances 28 and 31 occur between the terminals 5 and 6, and the switches 34 and 35 and the value of the inductances are primarily determined by lay-out and die mounting technique. The parasitic inductances 29 and 30 are provided between the terminal 7 and the switches 34 and 35, and the value of these inductances is likewise primarily determined by layout and die mounting technique.

Parasitic capacities 32 and 33 are provided in parallel with the switches 34 and 35, and the value of these capacities is determined by the manufacturing method used by the component supplier.

The parasitic capacities and inductances thus form an oscillation circuit, which is turned on by the switching terminal 7 between the terminals 5 and 6, which causes ringings on the terminals of the switched circuit. These ringings may be attenuated considerably by connecting the circuit 1 to the terminals 5 and 6. The switches in figure 3 are illustrated by two force-commutated contacts (transistors), but may also be formed by a force-commutated and a non-force-commutated contact (e.g. a diode).

Figure 4 shows an example of how the circuit 1 may be realized as a two-port network. The inductance 13 of the circuit is shown to be connected between the terminals 21 and 23, and the series coupling of the capacitor 14 and the resistor 15 of the circuit is shown to be connected between the terminals 23 and 24.

Figure 5 shows another example of how the circuit 1 may be realized as a two-port network, said two-port network

being provided with a resistor 16 in parallel with the inductance 13 between the terminals 21 and 23.

When using this embodiment of the two-port network, the value of the resistor 15 may be increased, as the resistors 15 and 16 form a parallel coupling at high frequencies. Optionally, the resistor 15 may be selected to be infinitely great, so that the capacitor 14 and the resistor 15 may be omitted completely. The terminals 22 and 24 are interconnected.

Figure 6 shows a course of the ringings immediately after the switching of the terminal 7, with and without the circuit 1 connected to the terminals 5 and 6. The AC course of the ringings for the terminal 7 is shown at 27 without the circuit 1 connected, and at 18 with the circuit 1 connected to the terminals 5 and 6. It will be seen that the ringings 27 are slightly attenuated, and thereby constitute a relatively great part of the switching period, which causes distortion of the pulse height and electromagnetic radiation. On the other hand 18 shows a very attenuated course of the ringings, and the transient constitutes less than a period in practical realizations, which means that the pulse height distortion and the electromagnetic radiation are very low.

Figure 7, at 18, shows an example of the AC course of the voltage across the resistor 15 immediately after the switching of the terminal 7 from the terminal 6 to the terminal 5, where the current into the terminal 7 has a positive sign. If the value of the resistor is selected such that critical attenuation of the serial oscillation circuit is obtained in the switched circuit, a course of the same type as given at 18 is obtained. Thus it is shown at 18 how the voltage across the resistor 15 increases very rapidly to a peak value, which is predominantly determined by the value of the resistor 15, multi-

plied by the current in the terminal 7. The voltage decreases as the current is taken over by the inductance 13, and is zero after a short transient. With the same conditions, 19 shows a sequence where the terminal 7 is switched from the terminal 5 to the terminal 6, and it will be seen that the current in the inductance 13 is switched from running in the terminal 5 to run in the capacitor 14 and the resistor 15, whereby the voltage across the resistor 15 assumes a negative value, which is given by the product of the value of the resistor 15 and the current in the inductance at the switching moment. The voltage then increases toward zero as the current in the inductance 13 decreases, and is zero after a short transient.

Figure 8 shows an example of how the circuit 1 may be realized with one two-port network as described in connection with figure 1 and 3. The terminals 21 and 22 of the two-port network are connected to the terminal 3 and the terminal 4, respectively, of the circuit 1, and the terminal 20 of the circuit is connected to the terminal 4. The terminals 23 and 24 of the two-port network are connected to the terminals 5 and 6, respectively, of the circuit.

Figure 9 shows another example of how the circuit 1 may be realized with two two-port networks, where the terminals 21 of the two-port networks are connected to the terminals 3 and 4, respectively, of the circuit 1, and where the terminals 22 of both two-port networks are connected to the terminal 20 of the circuit. The terminals 23 of the two-port networks are connected to the terminals 5 and 6, respectively, of the circuit.

Figure 10 shows an example of how the circuit 9 may be realized with a single voltage supply 24, which is connected between the terminals 3 and 4 of the circuit 9, and where the terminal 20 is connected to the terminal 4.

Figure 11 shows a further example of how the circuit 9 may be realized with a double voltage supply given by 24 and 25, where the voltage supply 24 is connected to the terminals 3 and 20 of the circuit 9, and the voltage supply 25 is connected to the terminals 20 and 4 of the circuit 9.

Figure 12 shows an example of how the circuit 9 may be realized with a load 26 which is connected between the terminals 3 and 4, and where the terminal 20 is connected to the terminal 4.

Figure 13 shows an example of how the circuits 1 and 2 on fig. 1 may be realised where the load can be connected between the terminals 7 and 8 and the power supply can be connected between the terminals 3 and 4.

Figure 14a - 14g illustrates different current flow graphs of the circuit shown in figure 13 where the current flow graph is split into 6 states of the circuits 1 and 3.

Figure 14a shows a state where the switch 35 is conducting a positive load current and the current is running in the snubber inductor 13 and the two parasitic inductors 30 and 31.

Figure 14b shows the same circuits 1 and 3 where the switch 35 just have been switched off and the switch 34 just have been switched on, due to that the current running in the snubber inductor 13 and the currents running in the parasitic inductors 30 and 31 can not change simultaneously the currents will run in the capacitor 14 and the resistor 15 until the inductors 13, 30 and 31 contained energies is zero. In realisation of circuit 1 and 3 the inductor 13 will typically be chosen to have an inductance much greater than the parasitic

inductance's together, which yields that the inductance 13 can be neglected at the resonance frequency of the parasitic components 28, 29, 30, 31, 32 and 33 and it is thereby seen that the resistor 15 damp's the ringings in the output stage.

Figure 14c shows the circuits 1 and 3 right after the energy in the parasitic inductors is zero and it is seen that load current is running through the switch 34 and its parasitic inductance's 28 and 29. Furthermore it is seen that the current that was in the inductor 13 still is running in the capacitor 14 and the resistor 15 until the energy in the inductor 13 is zero.

Figure 14d shows the circuits 1 and 3 in a state where the switching from switch 35 to switch 34 is finished and 34 is conducting a positive load current and the current is running in the switch 34 itself and in the two parasitic inductors 28 and 29.

Figure 14e shows the current flow in the circuit 1 and 3 under the switching of the load from switch 34 to switch 35 and it is seen that the current from the load is running in the capacitor 14 and the resistor 15 and that the resonant high frequency current running in the parasitic components 28, 29, 30 and 31 of the switches 34 and 35 also runs through the capacitor 14 and the resistor 15. The resonance frequency of the parasitic components 28, 29, 30, 31, 32 and 33 is thereby damped by the resistor 15.

Figure 14f shows the current flow in the circuit 1 and 3 after the switching from switch 34 to switch 35 is done and the load current is taken over from the capacitor 14 and the resistor 15 by the snubber inductor 13.

Figure 14g shows the following current flow of the circuits 1 and 3 and it is seen that the current flow is

id ntical to that in figure 14a and thereby is the current flow graph completed.

Figure 15a shows the current flow diagram for circuit 1 and 3 at low frequencies when the load i.e. terminal 7 is switched to the power supply i.e. terminal 3, and it is seen that the current path strictly is given by the switch 35.

Figure 15b shows the current flow diagram for circuit 1 and 3 at low frequencies when the load i.e. terminal 7 is switched to the ground terminal 4, and it is seen that the current path strictly is given by the switch 34.

Figure 16a shows the current flow diagram for circuit 1 and 3 at very high frequencies, right after the load is switched from switch 34 to switch 35, and it is seen that the current running in the parasitic components 28, 29, 30, 31, 32 and 33 primarily is running in the capacitor 14 and the resistor 15, and with the right values of the capacitor 14 and the resistor 15, the oscillation circuit consisting of the parasitic components 28, 29, 30, 31, 32 and 33 can thereby be damped effectively by the resistor 15.

Figure 16b shows the current flow diagram for circuit 1 and 3 at very high frequencies, right after the load is switched from switch 35 to switch 34, and it is seen that the current running in the parasitic components 28, 29, 30, 31, 32 and 33 primarily is running in the capacitor 14 and the resistor 15, and with the right values of the capacitor 14 and the resistor 15, the oscillation circuit consisting of the parasitic components 28, 29, 30, 31, 32 and 33 can thereby be damped effectively by the resistor 15.

As will be appreciated from the foregoing, the invention provides a circuit with low losses which, in combination

with a switched circuit of the two-port type, is capable of generating minimally distorted square-wave pulses with minimum noise and oscillations, and which is capable of limiting the peak current in the switches during the switching sequences, said circuit having a very low complexity.

Patent Claims:

1. A method of reducing distortion and noise of square-wave pulses and of limiting peak currents which occur during the switching sequences in switched circuits of the two-port type, which has a switchable port with a switching terminal capable of being switched between the terminals of a second circuit, characterized in that the terminals of the switched circuit are connected to a set of terminals on the second circuit, and that the second circuit is given a short-circuit impedance which, seen from the switched circuit, provides a characteristic which has a low impedance at low frequencies, while it has a high impedance and is predominantly resistive at high frequencies.

2. A method according to claim 1, characterized in that a single or double voltage supply is applied to the terminals of the second circuit which are not connected to the switched circuit, and that a series coupling of an inductance and a load circuit is applied to the port of the switched circuit containing the switching terminal.

3. A method according to claim 1, characterized in that a load circuit is connected to the terminals of the second circuit which are not connected to the switched circuit, and that a series coupling of an inductance and a voltage supply is applied to the port of the switched circuit containing the switching terminal.

4. A circuit of the type which, in combination with a switched circuit of the two-port system, is capable of generating minimally distorted square-wave pulses with minimum noise and of limiting peak currents which occur during the switching sequences of the square-wave pulses,

said switched circuit having a terminal capable of being switched between two terminals of a second circuit, c h a r a c t e r i z e d in that the second circuit is formed by a network which, seen from the switched circuit, has a short-circuit impedance which has a low impedance at low frequencies and has a high impedance and is predominantly resistive at high frequencies.

5. A circuit according to claim 4, c h a r a c t e r i z e d in that the port of the second circuit which is not switched by the switching circuit, is formed by two interconnected two-port networks.

6. A circuit according to claim 4 or 5, c h a r a c t e r i z e d in that the network comprises an inductive component which is connected to a series connection of a capacitive and a resistive component.

7. A circuit according to claim 6, c h a r a c t e r i z e d in that a resistive component is connected in parallel with the inductive component.

8. A circuit according to claim 6 or 7, c h a r a c t e r i z e d in that the values of the capacitive and inductive components of the network are at least four times greater than the values of the parasitic capacitive and inductive components of the switched circuit.

9. A circuit according to claims 6-8, c h a r a c t e r i z e d in that the resistive value of the network at high frequencies is twice the characteristic impedance of the overall parasitic inductance and the overall parasitic capacitance of the switched circuit.

10. A circuit according to claims 4-9, c h a r a c t e r i z e d in that the resistive value of the network is reduced in that a series coupling of a resistor and a capacitor is connected between the switching terminal and

a common terminal, and another series coupling of a resistor and a capacitor is connected between the two terminals which are not formed by the common terminals.

11. A circuit according to any one of claims 4-10, c h a r a c t e r i z e d in that the network and the switched circuit are formed as an integrated unit on a substrate.

12. A circuit according to claim 11, c h a r a c t e r i z e d in that a conductor path on the substrate forms the inductive component of the circuit.

13. A circuit according to any one of claims 4-12, c h a r a c t e r i z e d in that the series connection of the capacitive and resistive components is formed by a capacitor and its internal series resistance.

14. Use of a circuit according to any one of claims 4-13 in combination with the half-bridges in a class D amplifier for audio.

15. Use of a circuit according to any one of claims 4-12 in combination with the half-bridges of a switch mode power supply.

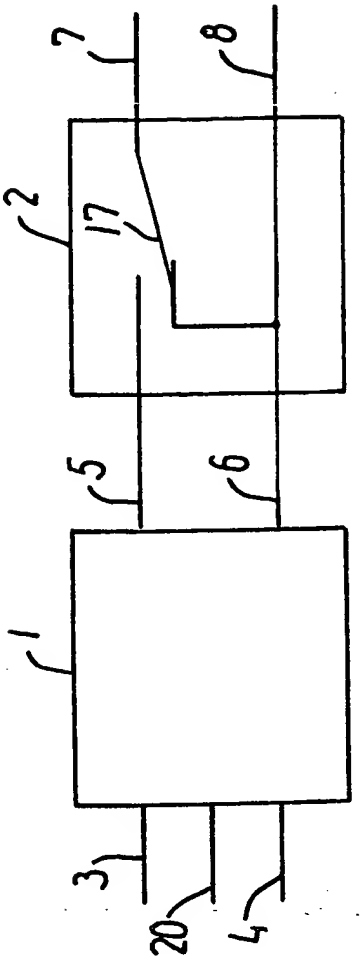

FIG.1

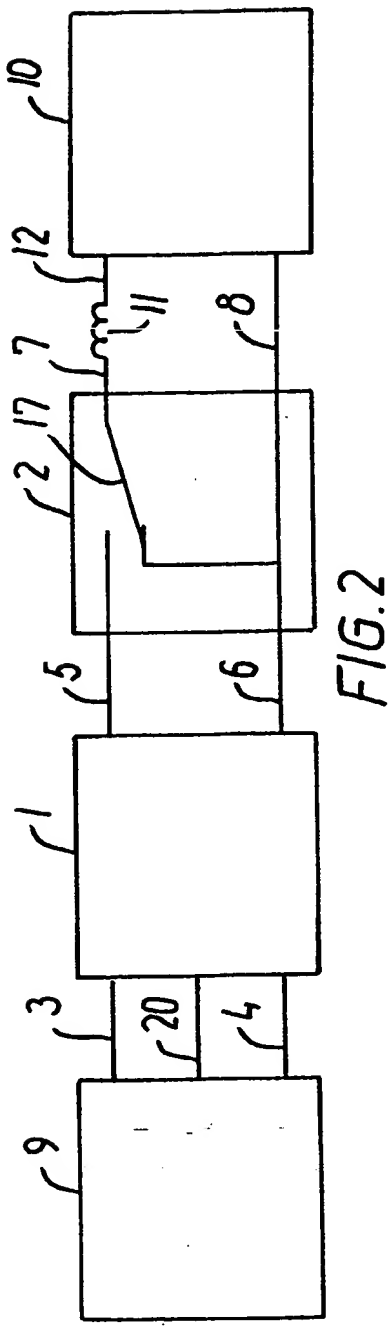

FIG.2

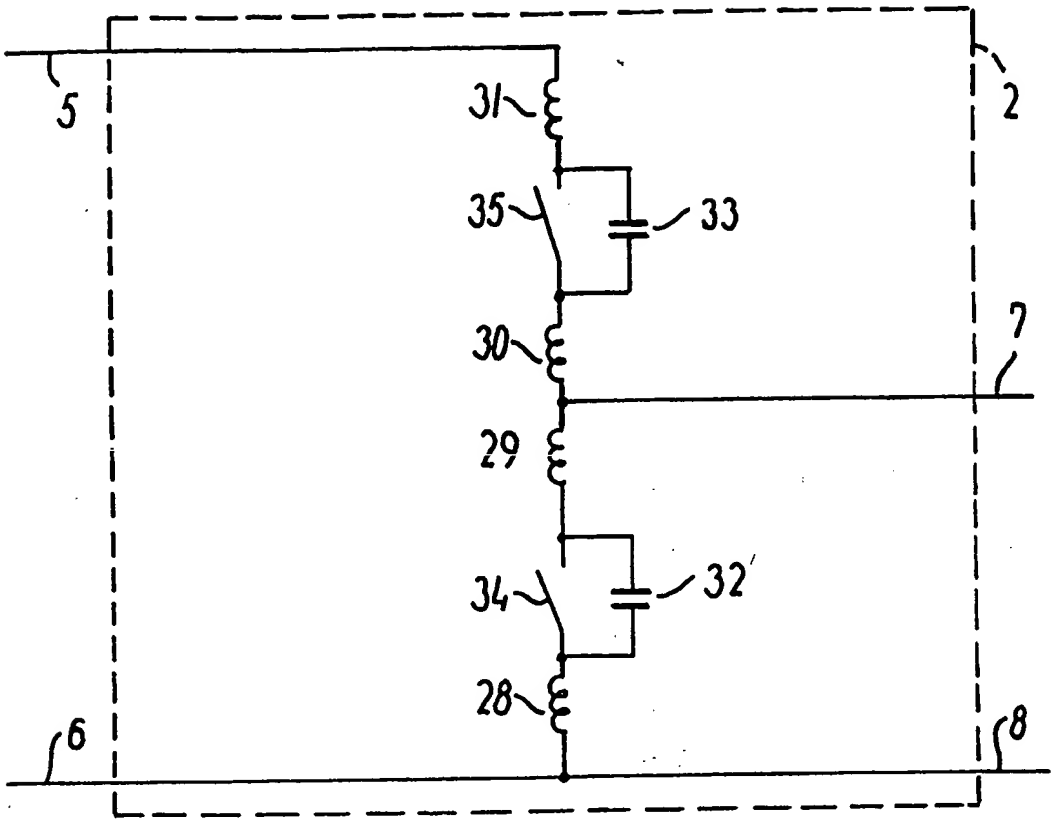

FIG. 2

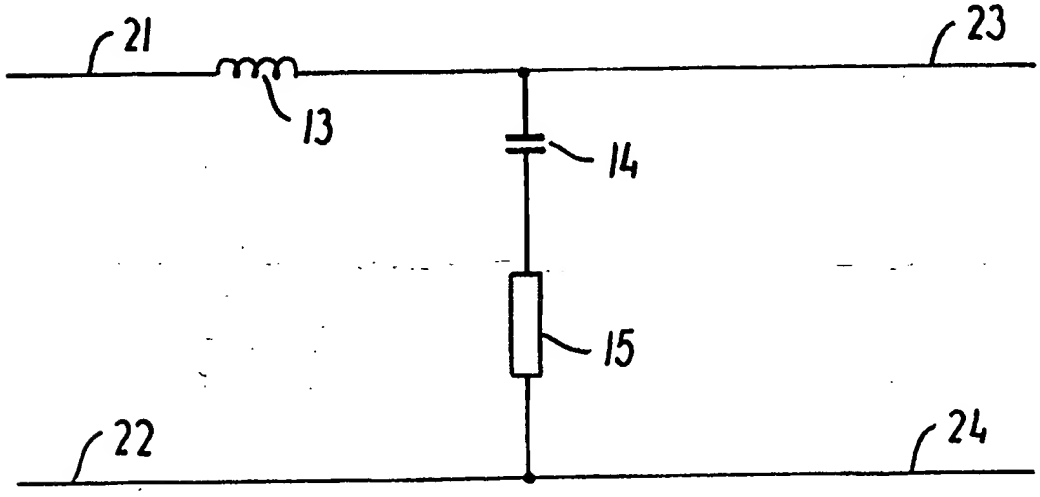

FIG. 4

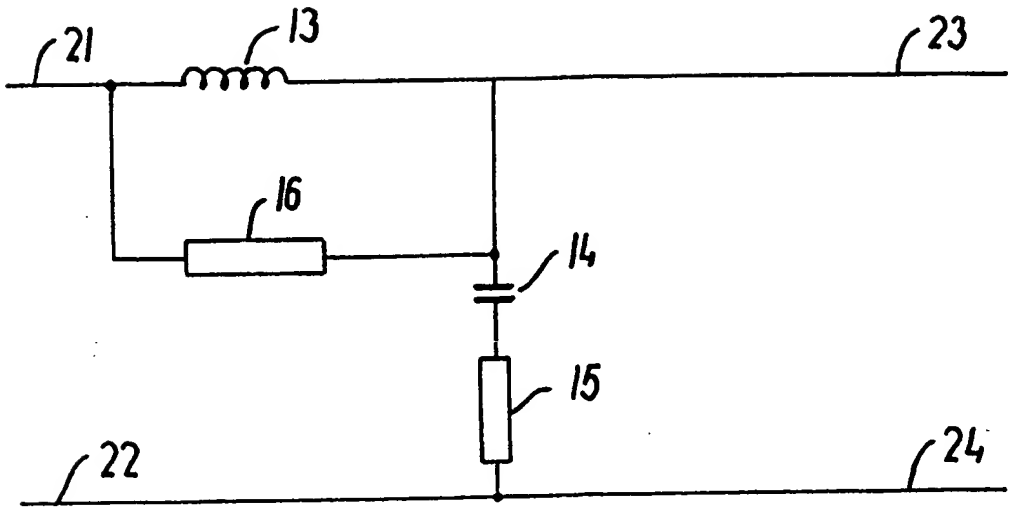

FIG.5

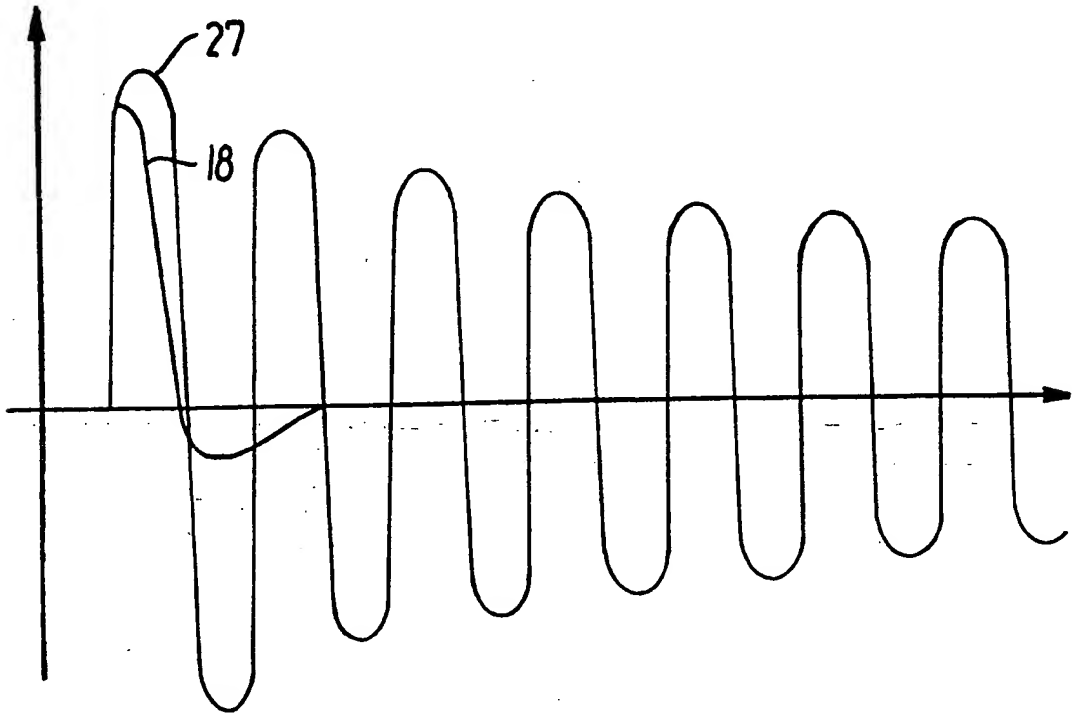

FIG.6

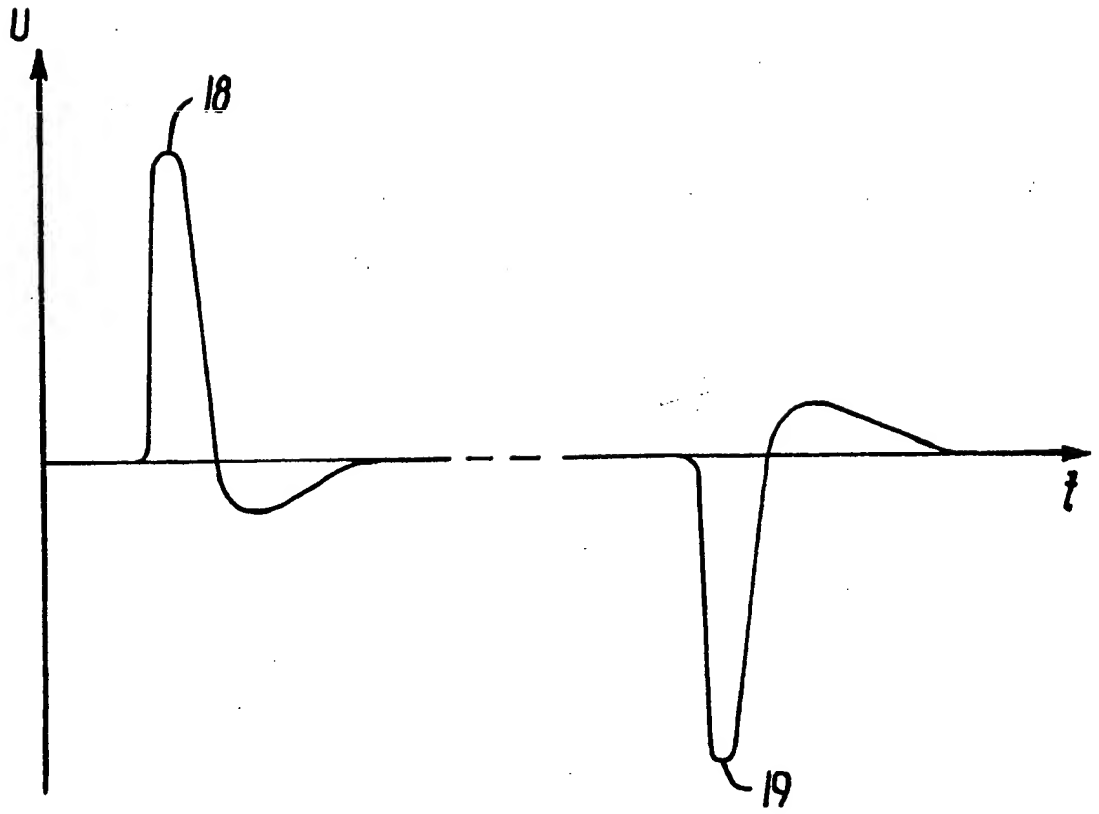

FIG.7

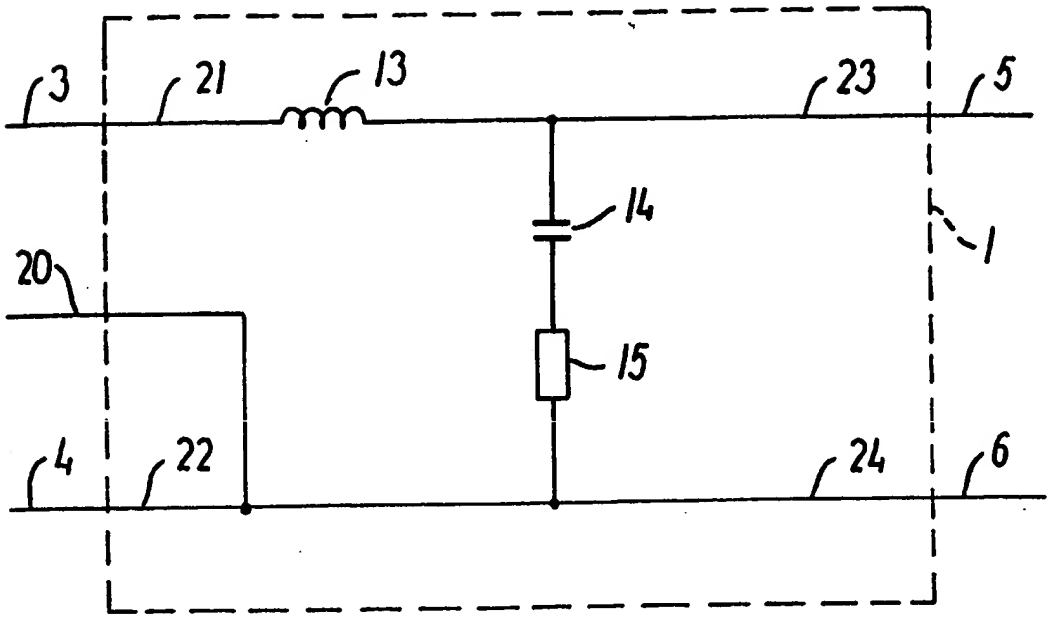
3
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FIG.8

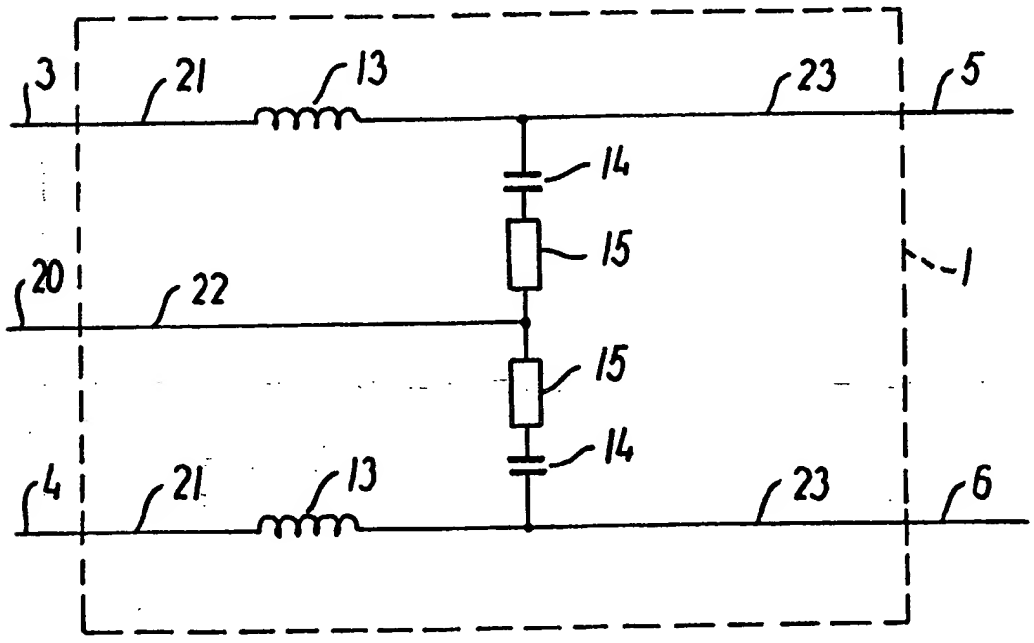
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FIG.9

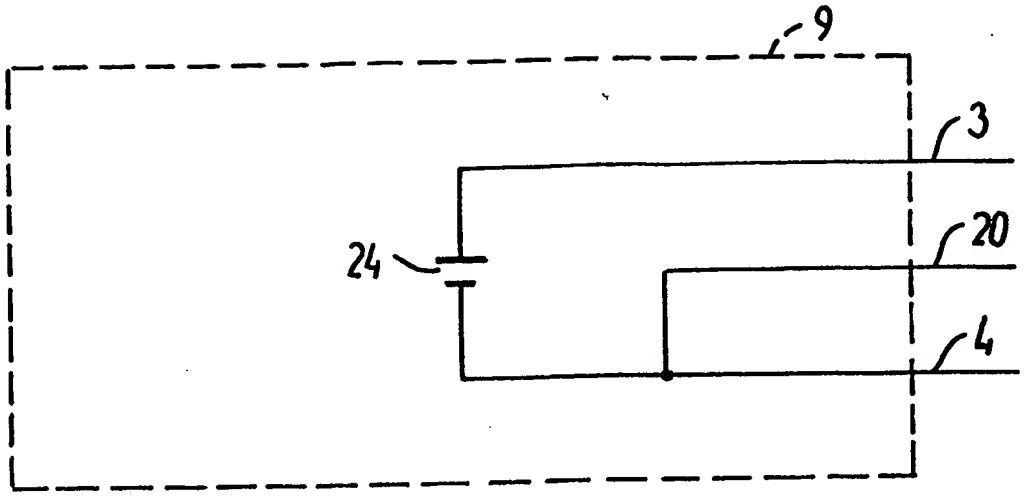

FIG. 10

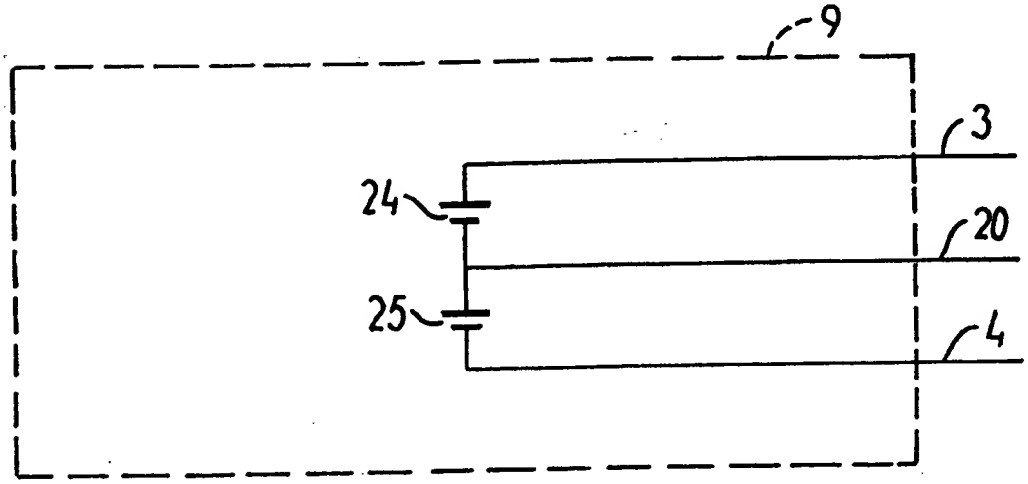

FIG. 11

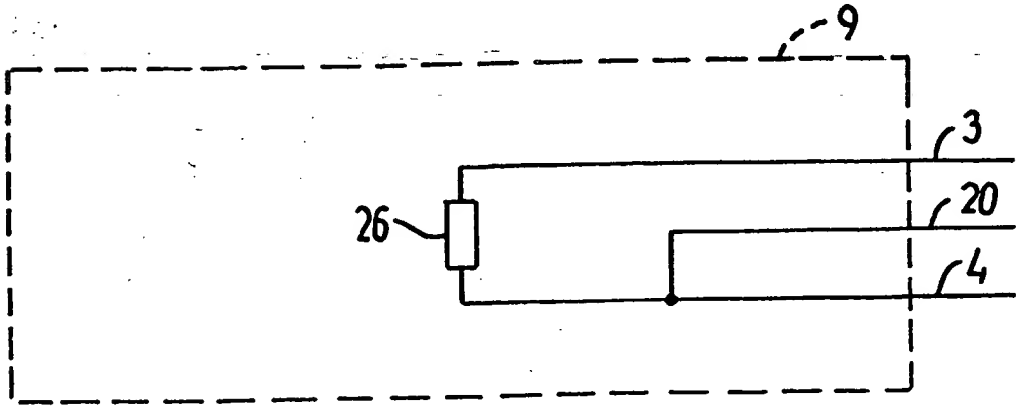

FIG. 12

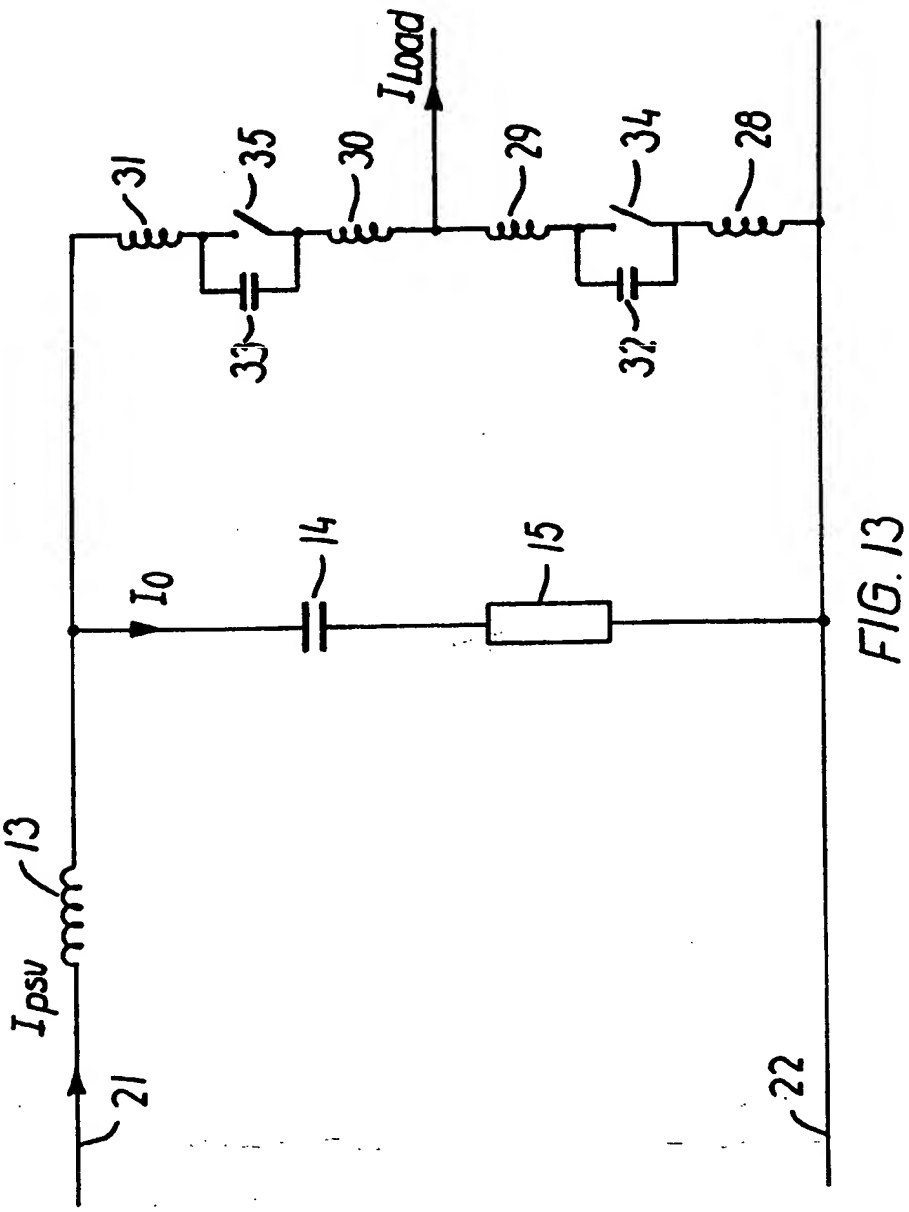

FIG. 13

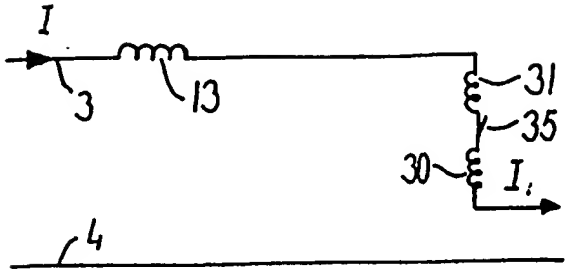

FIG. 14a

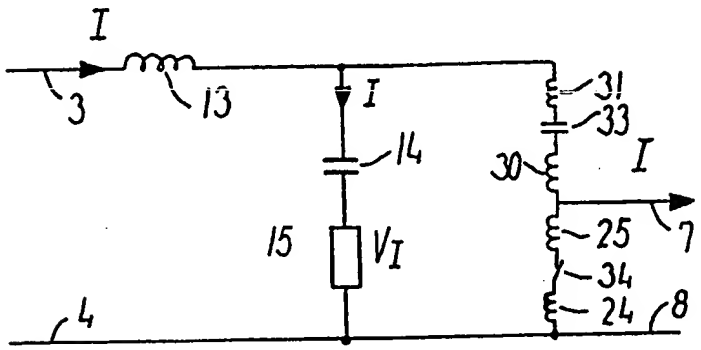

FIG. 14b

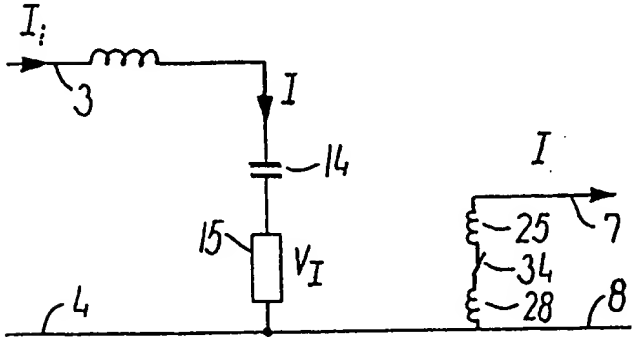

FIG. 14c

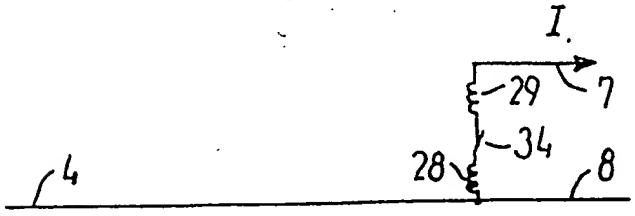

FIG. 14d

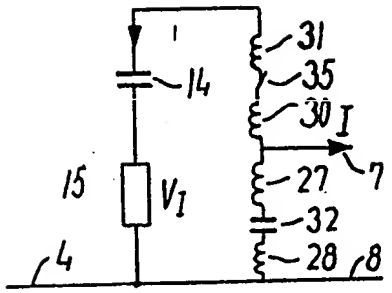

FIG. 14e

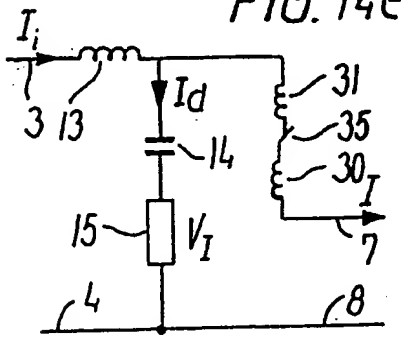

FIG. 14f

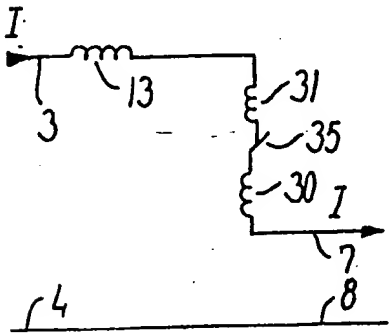

FIG. 14g

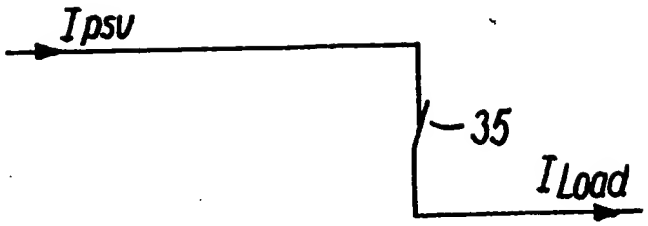

FIG. 15a

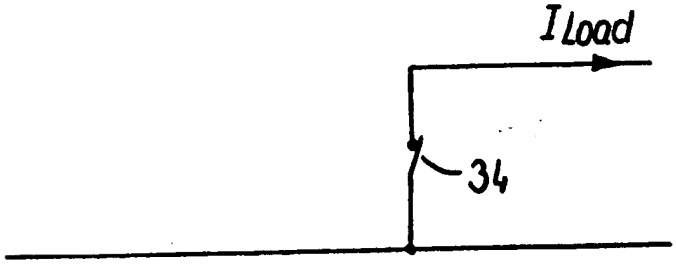

FIG. 15b

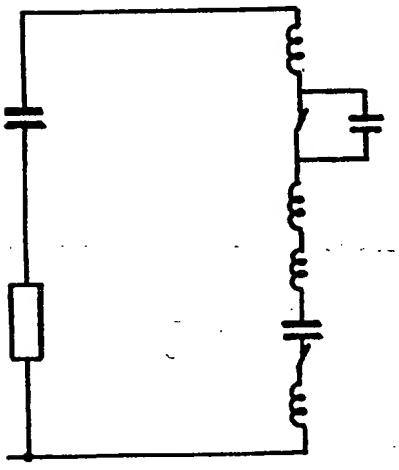

FIG. 16a

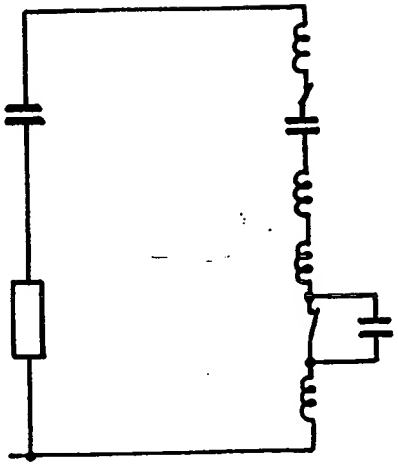

FIG. 16b

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(71) Applicant *(for all designated States except US)*: TOCCATA TECHNOLOGY [DK/DK]; Birkedommervej 27, 3, DK–2400 Copenhagen NV (DK).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: ANDERSKOUV, Niels [DK/DK]; Reventlovsgade 18, 4. tv, DK–1651 Copenhagen V (DK). RISBO, Lars [DK/DK]; Markmandsgade 14, 5. tv, DK–2300 Copenhagen S (DK).

(74) Agent: LINGPAT; v/ Ole Jagtboe, Køjevænget 56, DK–2791 Dragør (DK).

(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

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With international search report.

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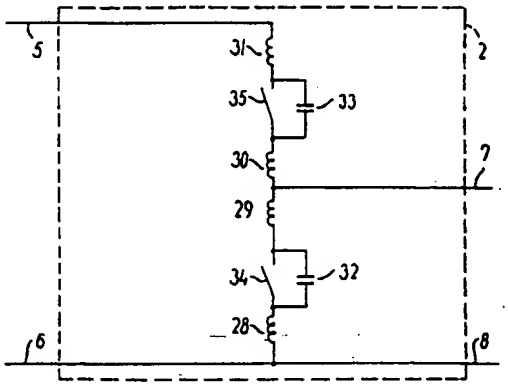
6 January 2000 (06.01.00)

(54) **Title:** A METHOD OF REDUCING DISTORTION AND NOISE OF SQUARE-WAVE PULSES, A CIRCUIT FOR GENERATING MINIMALLY DISTORTED PULSES AND USE OF METHOD AND CIRCUIT

(57) **Abstract**

With a view to generating minimally distorted square-wave pulses with limited noise and limited peak current during and after the switching sequences in a switched circuit, e.g. a class D amplifier output stage or a power supply, the invention provides a circuit and a method. Seen from one port of the circuit, the short-circuit impedance has a low impedance at low frequencies, while it has a high impedance and is predominantly resistive at high impedances. In one embodiment, the circuit consists of an inductance which is connected between the one and the other ports of the two-port network, and of a series connection of a resistor and a capacitor which is connected between the terminals of the other port of the circuit. The circuit, in combination with a switched circuit, may be formed as an integrated unit on a substrate, where the inductance may advantageously be formed by a conductor path.



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INTERNATIONAL SEARCH REPORT

International application No.
PCT/DK 99/00261

A. CLASSIFICATION OF SUBJECT MATTER

IPC6: H03F 3/217, H03F 1/56
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IPC6: H03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

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Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5506532 A (CIRO MILAZZO), 9 April 1996 (09.04.96), column 5, line 1 - line 64; column 9, line 8 - column 10, line 26	1,4-5
A		2-3,6-15
	--	
A	US 5917369 A (HUEY NGUYEN), 29 June 1999 (29.06.99), column 2, line 36 - line 60	1-15
	--	
A	US 5163174 A (HORST BEEKEN), 10 November 1992 (10.11.92), column 8, line 61 - column 9, line 39	1-15
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Name and mailing address of the ISA/ Swedish Patent Office Box 5055, S-102 42 STOCKHOLM Facsimile No. +46 8 666 02 86	Authorized officer Lotta Gunnarsson/AE Telephone No. +46 8 782 25 00

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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		DE 69317344 D,T	29/10/98
		EP 0590903 A,B	06/04/94
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		EP 0349743 A,B	10/01/90